ANALOG DEVICES

AN-720
APPLICATION NOTE

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AD8099 Evaluation Boards

by John Ardizzoni

INTRODUCTION

The AD8099 evaluation boards are designed to help customers quickly implement and evaluate new low noise, low distortion op amp designs. Any of the circuit configurations shown in the AD8099 data sheet can be fabricated using the AD8099 evaluation boards. The AD8099 evaluation boards have been designed for optimal performance and minimal layout parasitics.

There are two basic AD8099 evaluation board configurations: inverting and noninverting. These two configurations are offered for both package types, LFCSP and SOIC. Part numbers for the evaluation boards can be found in Table 7 of the AD8099 data sheet, or in Table 1 of this document.

The evaluation board features edge mounted SMA connectors at the input and output for efficient connection to other circuit boards or test equipment. The board is a 2-layer PCB, with ground plane on both sides of the board. The ground plane under the input pins has been removed. Removing the ground plane from under the input pins minimizes the stray capacitance at the input of the op amp, which improves stability and reduces peaking. The evaluation board components are SMTs and range from 0603 to 1206 case size; the electrolytic bypass capacitors (C1, C4), are 3528 case size.

Supply bypassing for the AD8099 is a key consideration for optimal circuit performance, especially when distortion is of concern. The AD8099 uses a combination of common-mode bypassing (a capacitor between the two power supplies) and shunt bypassing (from the power supply pins of the amplifier to ground). The evaluation board schematics show the bypassing schemes in detail, in Figures 1, 4, 7, and 10.

Since the AD8099 is externally compensated and has a large gain bandwidth product, the component values and placement are critical. The AD8099 data sheet features a detailed section on the compensation networks and component values. In low gain configurations (G = +2), the compensation network consists of three components, a series-parallel combination of resistor and capacitors to the negative supply. To minimize stray capacitance, the evaluation board provides only one set of mounting pads for the parallel components. Therefore, the parallel combination of resistor and capacitor (R7 and C_P for the SOIC boards and R_C, C_P for the LFCSP boards) must be soldered one on top of the other. Figure 13 illustrates the proper mounting configuration. The previously mentioned reference designators correspond to R_C and C1, found in the AD8099 data sheet.

The AD8099 output does not drive significant values of load capacitance (>5 pF); therefore the output connections should be kept short, direct, and terminated when appropriate. Minimizing the output capacitance will help ensure stability while minimizing peaking and ringing.

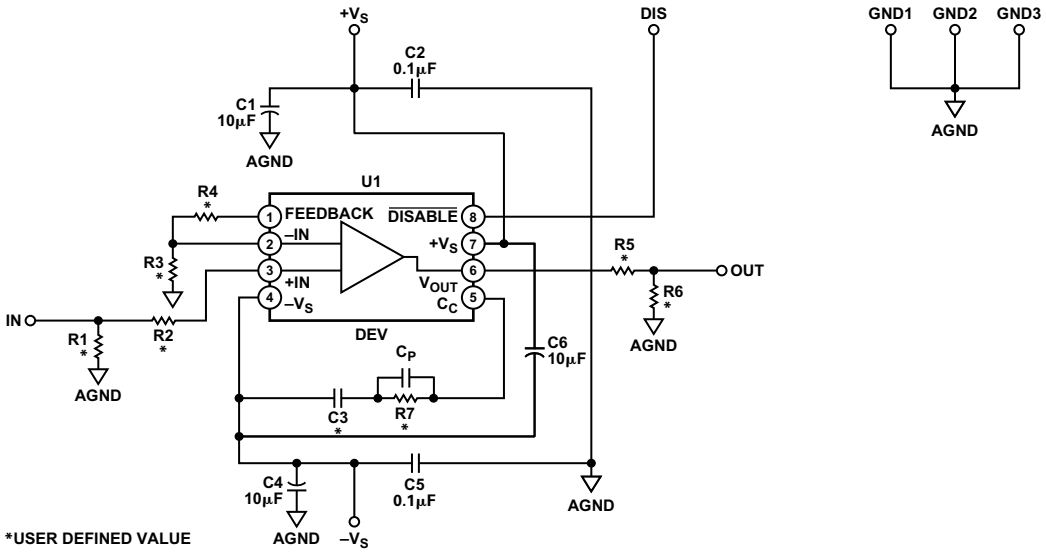

Figure 1. Noninverting Schematic (SOIC)

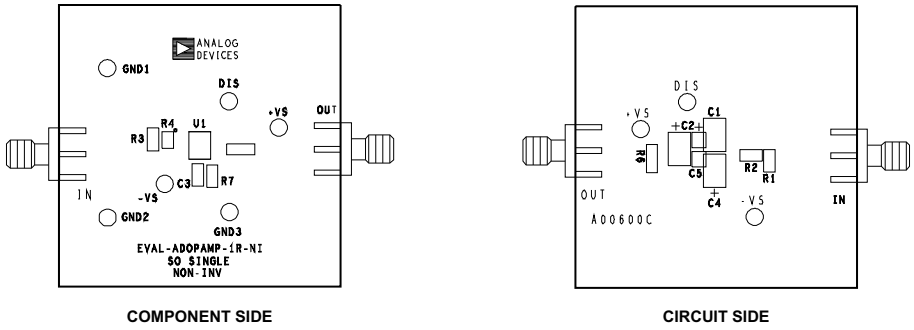

Figure 2. Board Assembly Drawings (SOIC)

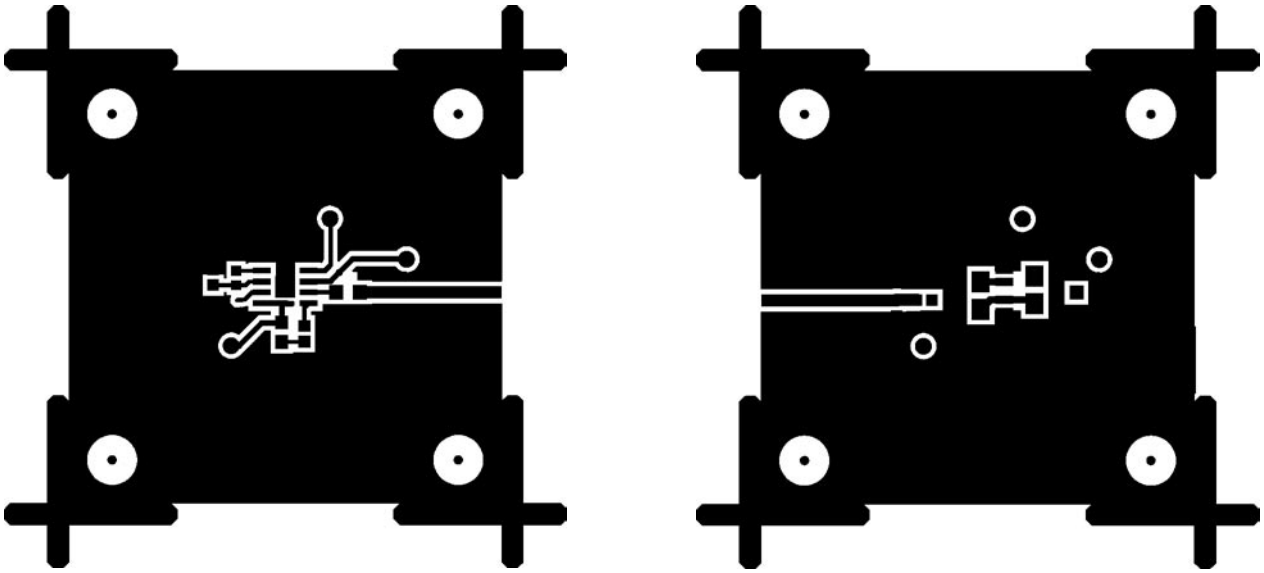

Figure 3. Board Layout Patterns (SOIC)

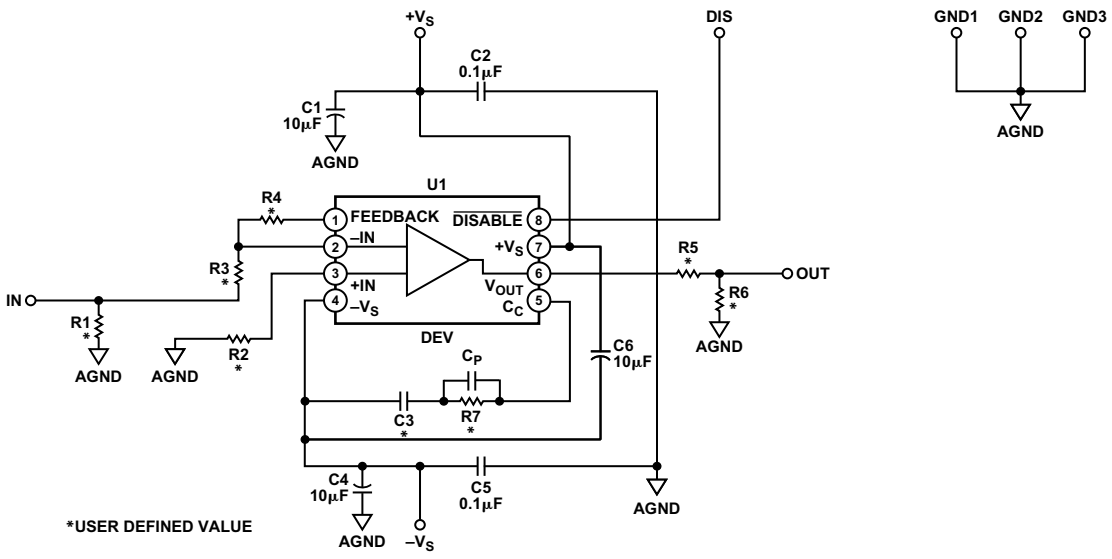

Figure 4. Inverting Schematic (SOIC)

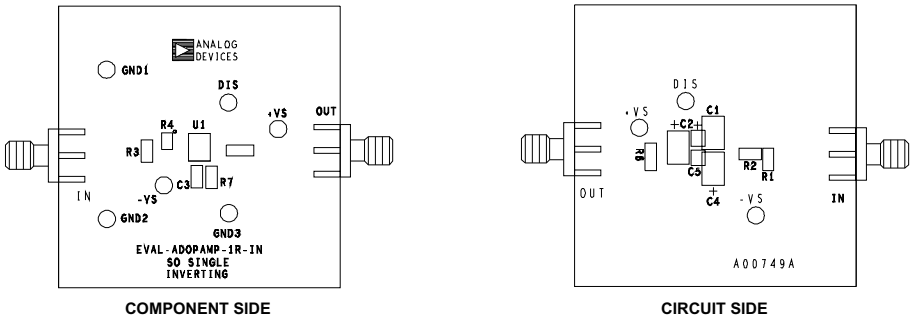

Figure 5. Board Assembly Drawings (SOIC)

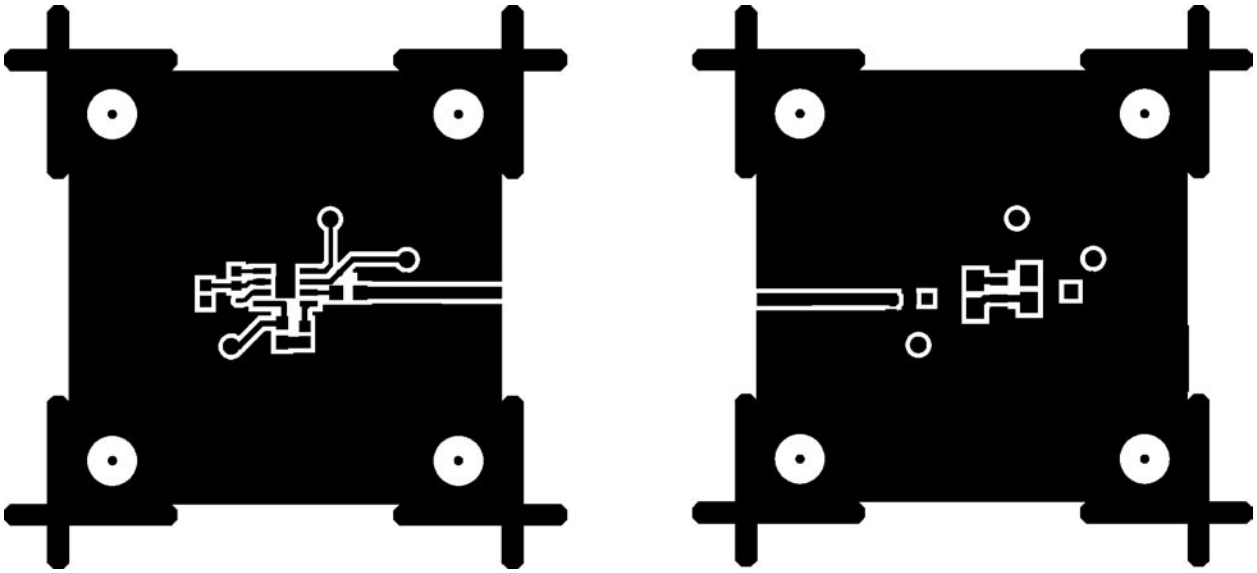

Figure 6. Board Layout Patterns (SOIC)

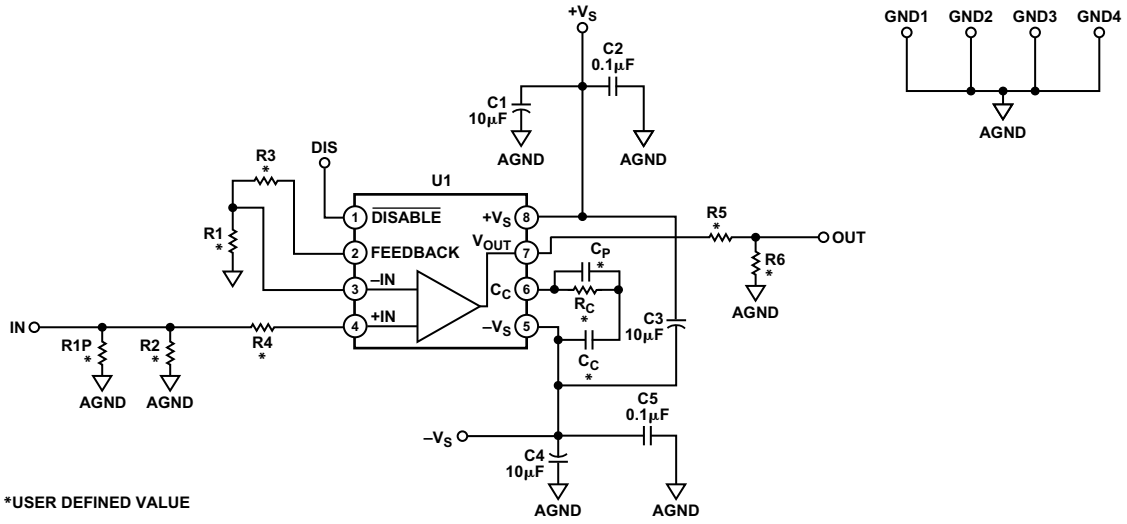

Figure 7. Noninverting Schematic (CSP)

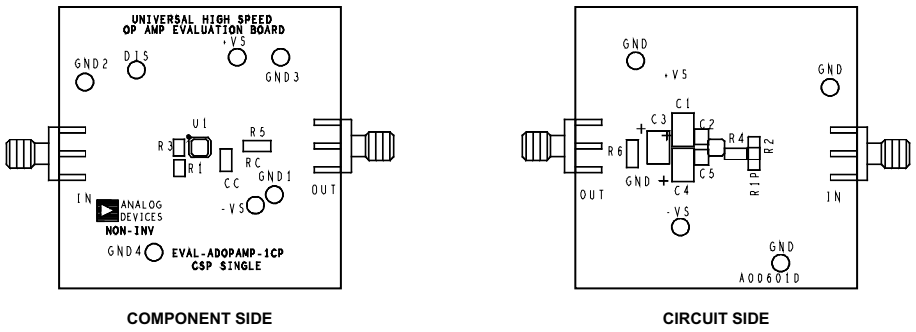

Figure 8. Board Assembly Drawing (CSP)

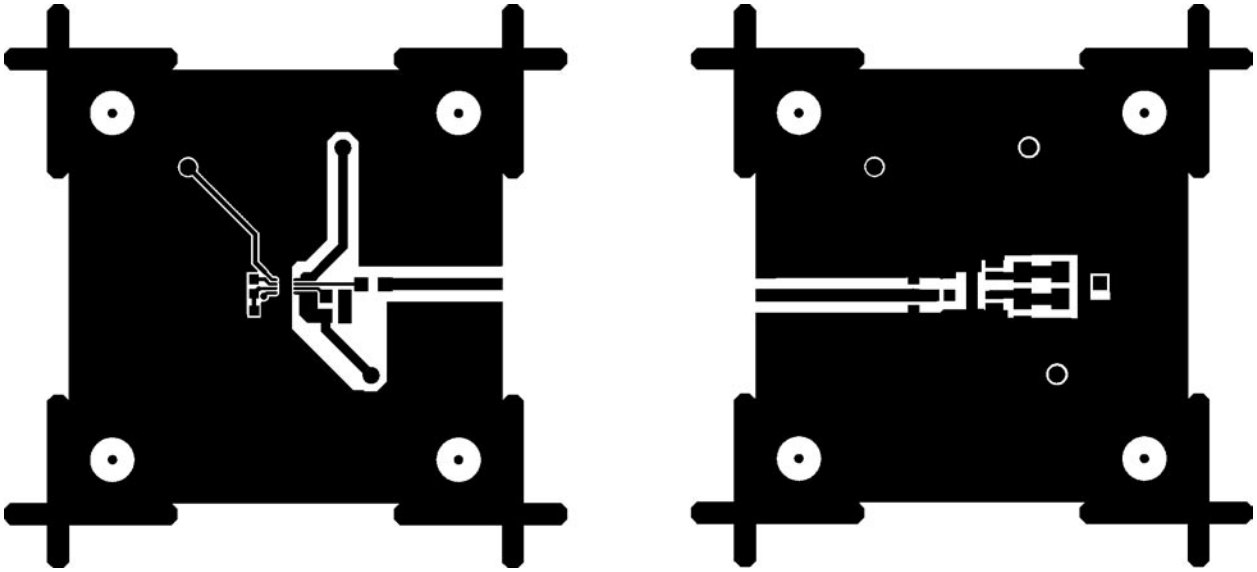

Figure 9. Board Layout Patterns (CSP)

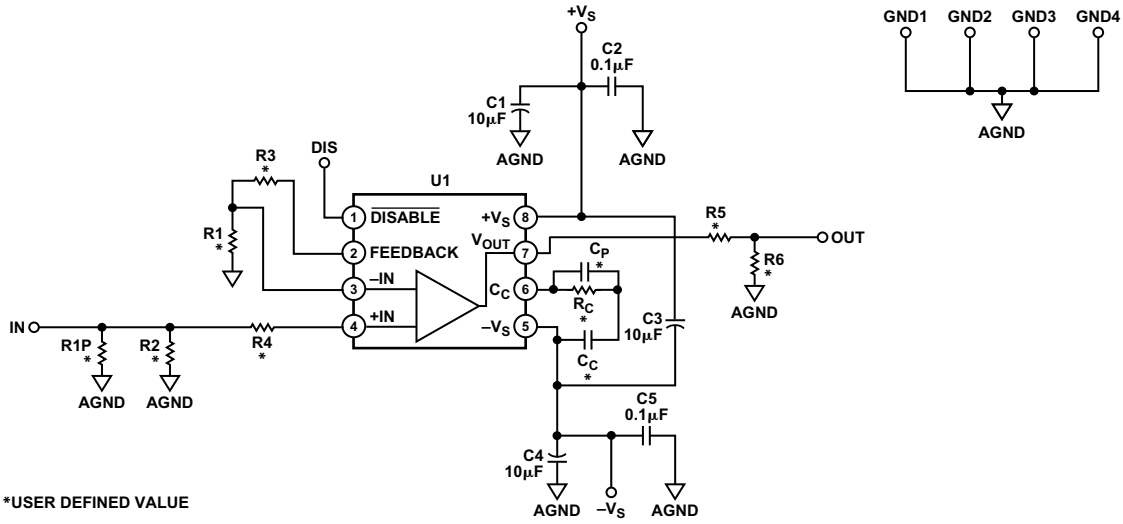

Figure 10. Inverting Schematic (CSP)

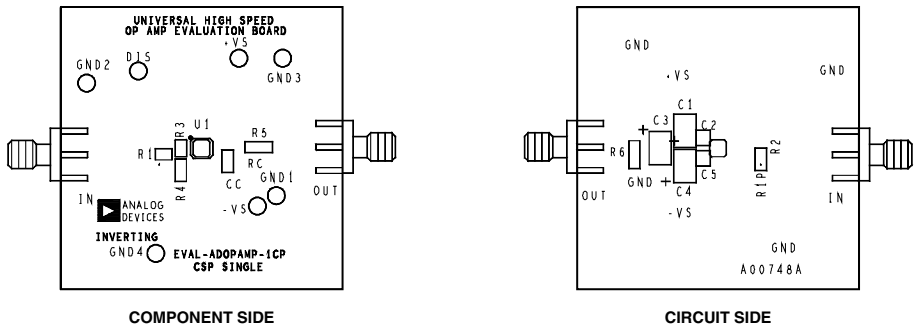

Figure 11. Board Assembly Drawing (CSP)

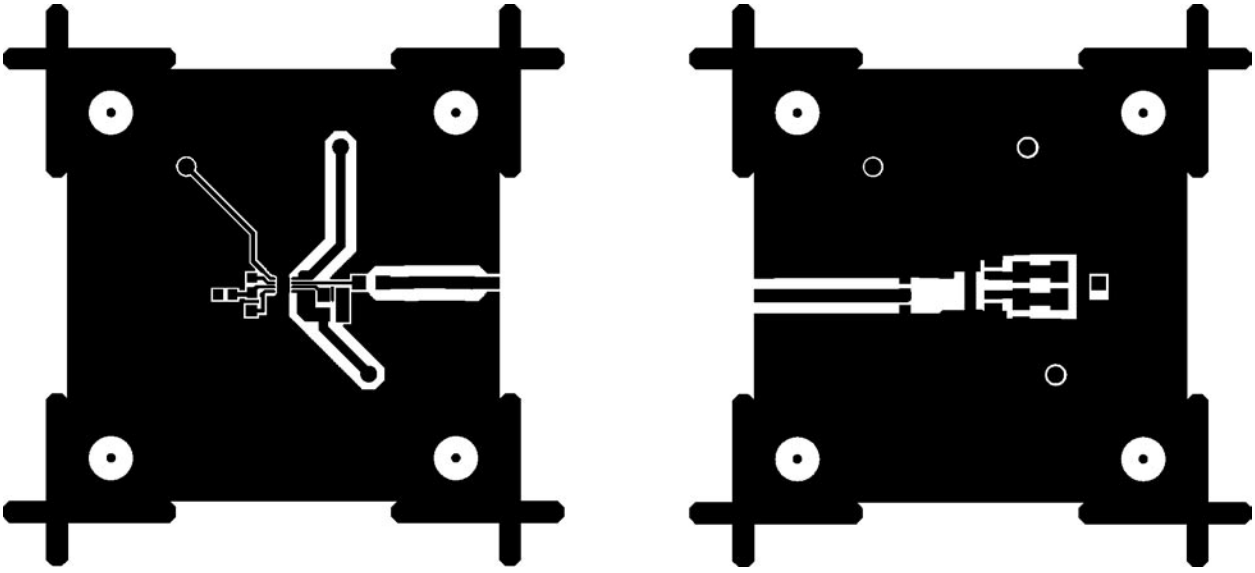

Figure 12. Board Layout Patterns (CSP)

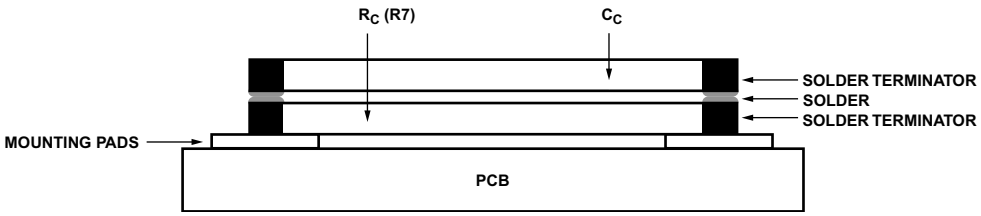

Figure 13. Soldering of Two Parallel Components

Table 1. Evaluation Board Selection Guide

	Package Type	
Board Configuration	**CSP**	**SOIC**
Inverting	EVAL-ADOPAMP-1CP-I	EVAL-ADOPAMP-1R-IN
Noninverting	EVAL-ADOPAMP-1CP-N	EVAL-ADOPAMP-1R-NI

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